Docket: GS 149

METHOD OF FORMING NARROW TRENCHES IN SEMICONDUCTOR SUBSTRATES

FIELD OF THE INVENTION

[0001] This invention relates to methods of forming narrow trenches in semiconductor substrates.

BACKGROUND OF THE INVENTION

[0002] Narrow trenches are commonly desired during fabrication of a wide array of semiconductor devices. Hence, although a specific example concerning the utility of narrow trenches is discussed below in connection with trench MOSFET devices, it is noted that narrow trenches have utility throughout the semiconductor field.

[0003] A trench MOSFET (metal-oxide-semiconductor field-effect transistor) is a transistor in which the channel is formed vertically and the gate is formed in a trench extending between the source and drain. The trench, which is lined with a thin insulator layer such as an oxide layer and filled with a conductor such as polysilicon (i.e., polycrystalline silicon), allows less constricted current flow and thereby provides lower values of specific on-resistance. Examples of trench MOSFET transistors are disclosed, for example, in U.S. Patent Nos. 5,072,266, 5,541,425, and 5,866,931, the disclosures of which are hereby incorporated by reference.

[0004] As a specific example, Figure 1 illustrates half of a hexagonally shaped trench MOSFET structure 21 disclosed in U.S. Patent No. 5,072,266. The structure includes an n+ substrate 23, upon which is grown a lightly doped n epitaxial layer 25 of a predetermined depth d_{epi}. Within the epitaxial layer 25, p body region 27 (p, p+) is provided. In the design shown, the p body region 27 is substantially planar (except in a central region) and typically lays a distance d_{min} below the top surface of the epitaxial layer. Another layer 28 (n+) overlying most of the p body region 27 serves as source for the device. A series of hexagonally shaped trenches 29 are provided in the epitaxial layer, opening toward the top and having a predetermined depth d_{tr}. The trenches 29 are typically lined with oxide and filled with conductive polysilicon, forming the gate for the

MOSFET device. The trenches 29 define cell regions 31 that are also hexagonally shaped in horizontal cross-section. Within the cell region 31, the p body region 27 rises to the top surface of the epitaxial layer and forms an exposed pattern 33 in a horizontal cross section at the top surface of the cell region 31. In the specific design illustrated, the p+ central portion of the p body region 27 extends to a depth d_{max} below the surface of the epitaxial layer that is greater than the trench depth d_{tr} for the transistor cell so that breakdown voltage is away from the trench surface and into the bulk of the semiconductor material.

[0005] A typical MOSFET device includes numerous individual MOSFET cells that are fabricated in parallel within a single chip (i.e., a section of a semiconductor wafer). Hence, the chip shown in Fig. 1 contains numerous hexagonal-shaped cells 31 (portions of five of these cells are illustrated). Cell configurations other than hexagonal configurations are commonly used, including square-shaped configurations. In a design like that shown in Fig. 1, the substrate region 23 acts as a common drain contact for all of the individual MOSFET cells 31. Although not illustrated, all the sources for the MOSFET cells 31 are typically shorted together via a metal source contact that is disposed on top of the n+ source regions 28. An insulating region, such as borophosphosilicate glass (not shown) is typically placed between the polysilicon in the trenches 29 and the metal source contact to prevent the gate regions from being shorted with the source regions. Consequently, to make gate contact, the polysilicon within the trenches 29 is typically extended into a termination region beyond the MOSFET cells 31, where a metal gate contact is provided on the polysilicon. Since the polysilicon gate regions are interconnected with one another via the trenches, this arrangement provides a single gate contact for all the gate regions of the device. As a result of this scheme, even though the chip contains a matrix of individual transistor cells 31, these cells 31 behave as a single large transistor.

[0006] Demand persists for trench MOSFET devices having ever-lower on-resistance. One way to reduce on-resistance is to increase cell density. Unfortunately, the gate charges associated with trench MOSFET devices also increase when cell density is increased. As a result, steps need to be taken to reduce such gate charges. As noted in JP05335582, the oxide film at the trench sidewall of a trench MOSFET device forms the channel within the P-body region. The oxide film at the bottom of the trench, on the

other hand, does not contribute significantly to channel formation, but nonetheless contributes to gate charges. The inventors in JP05335582 propose thickening the oxide film at the bottom of the trench substantially relative to the oxide film at the sidewall to reduce gate charges.

[0007] A related way to reduce the gate charge contribution of the trench bottoms is to provide narrower trenches, as is known in the art. The present invention provides a novel process for the formation of narrow trenches within a semiconductor substrate.

SUMMARY OF THE INVENTION

[0008] According to an embodiment of the invention, a method of forming a trench within a semiconductor substrate is provided. The method comprises: (a) providing a semiconductor substrate; (b) providing a patterned first CVD-deposited masking material layer having a first aperture over the semiconductor substrate; (c) depositing a second CVD-deposited masking material layer over the first masking material layer; (d) etching the second masking material layer until a second aperture that is narrower than the first aperture is created in the second masking material within the first aperture; and (e) etching the semiconductor substrate through the second aperture such that a trench is formed in the semiconductor substrate.

[0009] The first and second masking material layers are preferably of the same material composition (typically silicon oxide layers) and are preferably etched in anisotropic, dry oxide etching processes.

[0010] The substrate is preferably a silicon substrate and is preferably etched in an anisotropic, reactive ion etching process.

[0011] The first trench mask aperture can range, for example, from 0.4 to 0.8 microns across in smallest dimension, while the second trench mask aperture can range, for example, from 0.2 to 0.6 microns across in smallest dimension.

[0012] Preferably, the patterned first masking material layer is provided over the semiconductor substrate by a method comprising: (a) providing a first masking material layer over the semiconductor substrate; (b) applying a patterned photoresist layer (preferably a positive photoresist layer) over the first masking material layer; and (c)

etching the first masking material layer through an aperture in the patterned photoresist layer such that the first aperture is formed in the first masking material layer.

[0013] The method of the present invention is useful in forming trench MOSFET devices. According to one embodiment of the invention, a trench MOSFET device is formed by a method comprising: (a) providing a semiconductor wafer of first conductivity type; (b) depositing an epitaxial layer of first conductivity type over the wafer, the epitaxial layer having a lower majority carrier concentration than the wafer; (c) forming a body region of second conductivity type within an upper portion of the epitaxial layer; (d) providing a patterned first masking material layer over the epitaxial layer, the patterned first masking material layer comprising a first aperture; (d) depositing a second masking material layer over the first masking material layer; (e) etching the second masking material layer until a second aperture that is narrower than the first aperture is created in the second masking material layer within the first aperture; (f) forming a trench in the epitaxial layer by etching the semiconductor wafer through the second aperture; (g) forming an insulating layer lining at least a portion of the trench; (h) forming a conductive region within the trench adjacent the insulating layer; and (i) forming a source region of first conductivity type within an upper portion of the body region and adjacent the trench. Preferably, the semiconductor wafer and the epitaxial layer are formed from silicon, and the first and second masking material layers are preferably formed from silicon dioxide.

[0014] One advantage of the present invention is that trenches with narrow widths can be formed within a semiconductor substrate.

[0015] Another advantage of the present invention is that a trench MOSFET device can be formed with narrow trenches, and hence reduced gate charges.

[0016] Another advantage of the present invention is that trench masks can be formed having apertures that are smaller than those directly obtainable from photolithographic processing.

[0017] These and other embodiments and advantages of the present invention will become immediately apparent to those of ordinary skill in the art upon review of the detailed description and claims to follow.

BRIEF DESCRIPTION OF THE DRAWINGS

[0018] Fig. 1 is a schematic cross-sectional view of a trench MOSFET device in the prior art.

[0019] Figs. 2A through 2D are schematic cross-sectional views illustrating a process for forming a narrow trench, according to an embodiment of the present invention.

[0020] Figs. 3A and 3B are schematic cross-sectional views illustrating a method of increasing sidewall spacer width, according to an embodiment of the present invention.

[0021] Figs. 4A through 4C are schematic cross-sectional views illustrating a method of making a trench MOSFET device, according to an embodiment of the present invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS OF THE INVENTION

[0022] The present invention now will be described more fully hereinafter with frequent reference to the accompanying drawings, in which preferred embodiments of the present invention are shown. This invention may, however, be embodied in different forms and should not be construed as limited to the embodiments set forth herein.

[0023] According to an embodiment of the present invention, a semiconductor substrate is the preferred substrate. The semiconductor substrate can be any such substrate known in the art, including elemental semiconductor substrates, such as silicon or germanium, or compound semiconductor substrates, such as GaAs, AlAs, GaP, InP, GaAlAs, and so forth. The semiconductor substrate can be single crystal, polycrystalline and/or amorphous, and it can be doped or undoped. A specific example of a semiconductor substrate is presented in connection with Figs. 2A through 2D. Referring to Fig. 2A, a silicon semiconductor substrate 201 is shown, which consists of an N+ doped silicon wafer 200 having an N doped silicon epitaxial layer 202 disposed thereon.

[0024] Once the substrate is selected, a first layer of a masking material that is appropriate for forming a trench mask is provided on the substrate and patterned using any appropriate technique known in the art. For example, a first masking material layer

can be provided on the substrate, and an appropriately patterned photoresist layer can then be provided over the first masking material layer, followed by etching under conditions that etch the masking material but do not substantially etch the photoresist material (and also preferably do not substantially etch the substrate beneath the masking material). After this etching step, the first layer of masking material contains one or more first mask apertures. Preferred materials for the masking material include CVD deposited materials, such as nitrides (e.g., silicon nitride) and oxides (e.g., silicon dioxide).

[0025] Referring again to the specific example of Figs. 2A-2D for purposes of illustration, a patterned first masking material layer 203 of a silicon oxide (typically silicon dioxide) with initial apertures 205i is formed on the epitaxial layer 202 as seen in Fig. 2A. A preferred technique for providing such as patterned first mask oxide layer 203 is as follows: first, a silicon dioxide layer is provided by depositing a non-doped silica glass (NSG) layer using techniques well known in the art. The deposition of such a layer is typically followed by a high-temperature annealing step, during which step the silicon dioxide layer is densified. A patterned layer of photoresist material, such as a positive photoresist material, is then provided over the resulting first mask oxide layer (i.e., the densified NSG layer). Subsequently, the oxide layer is anisotropically etched through apertures in the patterned layer of photoresist material using a dry oxide etch as is known in the art, producing a patterned first mask oxide layer 203 with initial apertures 205i. Using well-established 0.5-micron semiconductor technology, for example, this step typically results in minimum reproducible initial apertures 205i of about 0.4 microns.

[0026] As a next step, an additional layer of masking material is provided over the patterned first masking material layer. This additional layer is then etched, typically under conditions similar to those used to etch the apertures in the first layer of masking material, until portions of the semiconductor substrate are exposed within the initial mask apertures. At the same time, unetched portions of the additional masking material layer remain within the initial trench mask apertures adjacent the sidewalls of the same. These remaining portions are referred to herein as "sidewall spacers".

[0027] Referring back to Figs. 2A-2D as a specific example, a further layer of NSG is deposited over the patterned first mask oxide layer 203 of Fig. 2A, followed by densification, to form an additional mask oxide layer 203'. This mask oxide layer 203' is

then anisotropically **etched**, for example by using a dry oxide etch, until portions 202p of the epitaxial layer 202 are exposed, along with upper portions of the patterned first mask oxide layer 203, as shown in Fig. 2C. This etching process leaves behind sidewall spacer portions 203s, formed from the additional mask oxide layer 203', which are adjacent to the sidewalls of the initial apertures 205i. In this way, a "two-component" masking layer consisting of both the patterned first mask oxide layer 203 and sidewall spacers 203p is formed. This two-component masking layer contains final apertures 205f that are substantially narrower than the initial apertures 205i. In the case where initial apertures 205i are provided at the limit of the photolithographic technology available, the present invention provides a way of creating final mask apertures 205f that are beyond this limit. Using 0.5-micron technology as an example, final mask apertures 205f of about 0.2 microns can be produced.

[0028] An embodiment of the present invention in which the widths of the sidewall spacers 203s (and consequently the dimension of the final aperture 205f) can be varied will now be discussed. In this embodiment, the widths of the sidewall spacers 203 are increased by increasing the thickness of the patterned first mask oxide layer 203. This effect is illustrated in Figs. 3A and 3B in which two initial trench mask apertures 205i of the same width are produced within patterned mask oxide layers 203. Subsequently, an additional layer of masking material is provided and etched as described above, producing sidewall spacers 203s. The patterned mask oxide layer 203 in Fig. 3A is substantially thinner than the patterned mask oxide layer 203 in Fig. 3B. Under these circumstances, and because the profiles of the sidewall spacers 203s are relatively similar (from a geometric standpoint) in shape, the widths w of the sidewall spacers in Fig. 3A are substantially smaller (and hence the apertures 205f are substantially larger) than those in Fig. 3B.

[0029] Once the two-component trench mask is formed in accordance with the present invention, the semiconductor substrate is etched through the final apertures in the mask using an etching process by which the semiconductor material is selectively etched relative to the trench mask.

[0030] Referring once again to the specific example of Figs. 2A-2D, the silicon

epitaxial layer 202 is anisotropically etched, for example by reactive ion etching, through the final apertures 205f in the two-component oxide mask (which includes both the patterned first mask oxide layer 203 and the sidewall spacers 203s), resulting in trenches 207 as shown in Fig. 2D. The widths of the trenches 207 reflect the final apertures 205f, rather than the initial apertures 205i.

[0031] As noted above, narrow trench widths are useful in connection with trench MOSFET devices in that the gate-drain charges associated with such devices are reduced, among other effects. A method of forming a typical trench MOSFET device that incorporates the two-component trench mask of the present invention is briefly discussed here in connection with Figs. 4A-4C.

[0032] Turning now to Fig. 4A, an N doped epitaxial layer 202 is initially grown on an N+ doped substrate 200. A P-type region 204 is then formed in upper portion of the epitaxial layer 202 by implantation and diffusion. Subsequently, a two-component trench mask including both a patterned mask oxide layer 203 and oxide sidewall spacer portions 203s is formed as discussed above in connection with Figs. 2A-2C. The resulting structure is shown in Fig. 4A.

[0033] Trenches are then etched as discussed in connection with Fig. 2D above. Discrete P-type regions 204 are established as a result of this trench-forming step. The two-component trench mask is then removed and an oxide layer 210 is grown over the surface of the device, typically by dry oxidation at elevated temperature. Portions of the oxide layer 210 ultimately form the gate oxide regions for the finished device. The surface of the structure is then covered, and the trenches are filled, with a polysilicon layer, typically using CVD. The polysilicon is typically doped N-type to reduce its resistivity. The polysilicon layer is then etched, forming polysilicon gate regions 211. The resulting structure is shown in Fig. 4B.

[0034] Subsequently, n+ source regions 212 are formed in upper portions of the epitaxial layer via an implantation and diffusion process. BPSG (borophosphosilicate glass) regions 216 are then formed, typically by deposition, masking and etching processes, covering polysilicon regions 211 and a portion of the oxide regions 210. Finally, a metal contact layer (e.g., aluminum) is deposited, forming source contact 218.

The resulting structure is shown in Fig. 4C. A separate metal gate contact is also typically connected to a gate runner portion of the polysilicon that is located outside of the cell region of the trench MOSFET (not shown). Furthermore, a metal drain contact is also typically provided in connection with the semiconductor substrate (not shown).

[0035] Although various embodiments are specifically illustrated and described herein, it will be appreciated that modifications and variations of the present invention are covered by the above teachings and are within the purview of the appended claims without departing from the spirit and intended scope of the invention.